

# SPECIFICATION VER. 1.0



## **Revision History**

| Rev. | Description of change | Date        | Originator |
|------|-----------------------|-------------|------------|
| 1.0  | First creation        | 13. 01. 18. | KD PARK    |





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#### 1 Features

#### 1.1 General Features

- 4-Channel capacitive sensor with auto sensitivity calibration
- Selectable output operation mode (single output /multi output)
- Uniformly adjustable 9 step sensitivity
- Sync function for parallel operation
- 3 SYNC pins for various option selections
- Almost no external component needed
- Open-drain digital output
- Low current consumption
- Embedded common and normal noise elimination circuit
- RoHS compliant 14 SOP package

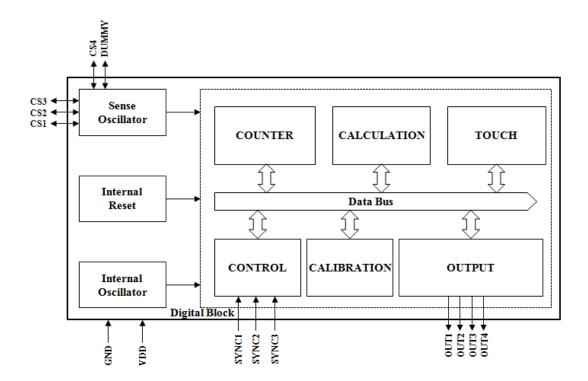
#### 1.2 Applications

- Home application
- Membrane switch replacement
- Sealed control panels, keypads
- Door key-lock matrix application
- Touch screen replacement application



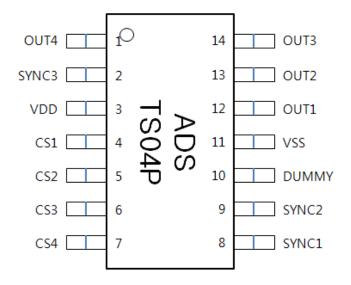


### 2 Block Diagram





## 3 Pin Configuration



[14-SOP]



### 4 Pin Description

#### 4.1 Pin Map

| Pin<br>Number | Name  | I/O                      | Description  | Protection |
|---------------|-------|--------------------------|--|------------|
| 1             | OUT4  | Digital Output           | CH4 parallel output (Open drain)                                       | VDD/GND    |
| 2             | SYNC3 | Digital Input<br>/Output | Output mode selection input <sup>1</sup><br>Sync pulse input /output 3 | VDD/GND    |
| 3             | VDD   | Power                    | Power (2.5V~5.0V)  | GND        |
| 4             | CS1   | Analog Input             | CH1 capacitive sensor input  | VDD/GND    |
| 5             | CS2   | Analog Input             | CH2 capacitive sensor input  | VDD/GND    |
| 6             | CS3   | Analog Input             | CH3 capacitive sensor input  | VDD/GND    |
| 7             | CS4   | Analog Input             | CH4 capacitive sensor input  | VDD/GND    |
| 8             | SYNC1 | Digital Input<br>/Output | Sensitivity selection input 1 <sup>2</sup> Sync pulse input /output 1  | VDD/GND    |
| 9             | SYNC2 | Digital Input<br>/Output | Sensitivity selection input 2 <sup>3</sup> Sync pulse input /output 2  | VDD/GND    |
| 10            | DUMMY | -                        | No Connection <sup>4</sup>   | VDD/GND    |
| 11            | VSS   | Ground                   | Supply ground  | VDD        |
| 12            | OUT1  | Digital Output           | CH1 parallel output (Open drain)                                       | VDD/GND    |
| 13            | OUT2  | Digital Output           | CH2 parallel output (Open drain)                                       | VDD/GND    |
| 14            | OUT3  | Digital Output           | CH3 parallel output (Open drain)                                       | VDD/GND    |

<sup>&</sup>lt;sup>4</sup> DUMMY pin should be no connection.



<sup>&</sup>lt;sup>1</sup> Refer to 8.3.3. Output mode selections.

<sup>&</sup>lt;sup>2</sup> Refer to 8.3.2. Sensitivity selections.

<sup>&</sup>lt;sup>3</sup> Refer to 8.3.2. Sensitivity selections.



### 5 Absolute Maximum Rating

Battery supply voltage6VMaximum voltage on any pinVDD+0.3Maximum current on any PAD100mAPower Dissipation800mWStorage Temperature $-50 \sim 150 \,^{\circ}C$ Operating Temperature $-20 \sim 75 \,^{\circ}C$ Junction Temperature $150 \,^{\circ}C$ 

Note: Unless any other command is noted, all above are operated in normal temperature.

### 6 ESD & Latch-up Characteristics

#### **6.1** ESD Characteristics

| Mode  | Polarity  | Max   | Reference            |  |
|-------|-----------|-------|----------------------|--|
|       | Pos / Neg | 7500V | VDD                  |  |
| H.B.M |           | 7500V | VSS                  |  |
|       |           | 7500V | P to P               |  |
|       | Pos / Neg | 550V  | VDD                  |  |
| M.M   |           | 550V  | VSS                  |  |
|       |           | 550V  | P to P               |  |
| C.D.M | -         | 1000V | Field Induced Charge |  |

#### **6.2** Latch-up Characteristics

| Mode               | Polarity | Max    | Reference |
|--------------------|----------|--------|-----------|
| I Toot             | Positive | 100mA  |           |
| I Test             | Negative | -100mA | JESD78A   |
| V supply over 5.0V | Positive | 8.25V  |           |





#### 7 Electrical Characteristics

■  $V_{DD}$ =3.3V, (Unless otherwise noted),  $T_A$  = 25 °C

| Characteristics                           | Symbol           | <b>Test Condition</b>       | Min | Тур | Max | Units |
|---|------------------|-----------------------------|-----|-----|-----|-------|
| Operating supply voltage                  | $V_{DD}$         |                             | 2.5 | 3.3 | 5.5 | V     |
| Comment assumention                       | т                | $V_{DD} = 3.3V$             | -   | 90  | 140 |       |
| Current consumption                       | $I_{DD}$         | $V_{DD} = 5.0V$             | -   | 110 | 180 | μΑ    |
| Internal reset criterion $V_{DD}$ voltage | $V_{DD\_RST}$    | $T_A = 25$ °C               | -   | 1.5 |     | V     |
| Output maximum sink current               | I <sub>OUT</sub> | T <sub>A</sub> = 25 °C      | -   | -   | 4.0 | mA    |
| Minimum detective capacitance difference  | $\Delta C_{MIN}$ |                             | 0.1 | -   | ı   | рF    |
| Output impedance                          | Zo               | $\Delta C > \Delta C_{MIN}$ | ı   | 12  | ı   | Ω     |
| (open drain)                              | 20               | $\Delta C < \Delta C_{MIN}$ | -   | 30M | -   | 32    |
| Self calibration time after system reset  | $T_{CAL}$        | Normal calibration speed    | -   | 80  | -   | ms    |

Note 1: The sensitivity can be decreased with higher parallel capacitance of CS pin including parasitic capacitance made by neighbor GND or other pattern.

Note 2: The series resistor (under  $1k\Omega$ ) of CS can be used in noisy condition to avoid mal-function from external surge and ESD.

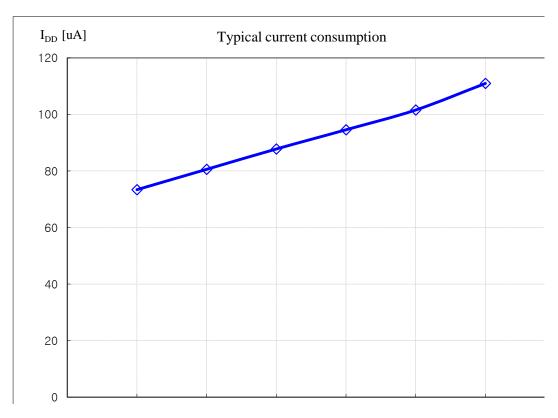




#### 8 TS04P Implementation

#### 8.1 Typical current consumption

TS04P uses internal bias circuit, so internal clock frequency and current consumption is fixed and no external bias circuit is needed. The typical current consumption curve of TS04P is represented in accordance with  $V_{\rm DD}$  voltage as below. Internal bias circuit can make the circuit design simple and reduce external components.



Typical current consumption curve of TS04P

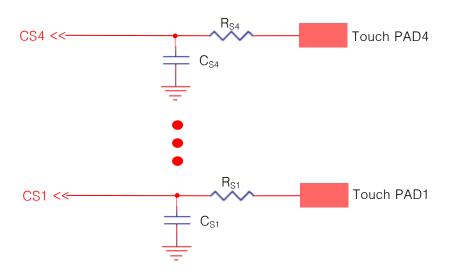
#### 8.2 CS implementation

TS04P has 9 step selections of sensitivity and internal protection circuit so external components of CS pins such as series resistor or parallel capacitor isn't necessary. The parallel parasitic capacitance of CS pins caused by touch line, touch pad and neighbor GND or other pattern may affect sensitivity. The sensitivity will be decreased when bigger parallel parasitic capacitance of CS pin is added.

Parallel capacitor ( $C_{S1\sim S4}$ ) of CS pin is useful in case of detail sensitivity mediation is required such as for complementation sensitivity difference between channels. Same as above parallel parasitic capacitance, sensitivity will be decreased when a big value of parallel capacitor ( $C_{S1\sim S4}$ ) is used. Under 50pF capacitor can be used as sensitivity mediation capacitor and a few pF is usually used. The  $R_S$ , serial connection resistor of CS pins, may be used to avoid mal-function from external surge and ESD. (It might be optional.) From 200 $\Omega$  to  $1k\Omega$  is recommended for  $R_S$ . Refer to below CS pins application figure.







The TS04P has eight independent touch sensor input from CS1 to CS4. The internal touch decision process of each channel is separated from each other. Therefore eight channel touch key board application can be designed by using only one TS04P without coupling problem.

The size and shape of PAD might have influence on the sensitivity. The sensitivity will be optimal when the size of PAD is approximately an half of the first knuckle (it's about 10 mm × 7 mm). The connection line of CS to touch PAD is recommended to be routed as short as possible to prevent from abnormal touch detect caused by connection line. The unused CS pin must be connected with the ground to prevent the unpredictable malfunction that occurred in the floating CS pin.

#### 8.3 SYNC implementation

The TS04P has five SYNC pins to make it possible to operate with many optional functions such as SYNC<sup>TM</sup> function, sensitivity selections, output mode selection, output level selection, and calibration speed selection. No external component is used for above selections.

The determination of SYNC pins connection of TS04P is accomplished in initial operation periods. Therefore changing connection of SYNC pin after initial operation period cannot affect the optional function selection.

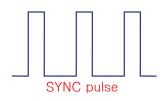
#### 8.3.1 SYNC<sup>TM</sup> function

For SYNC<sup>TM</sup> function, all SYNC pins (form SYNC1 to SYNC3) have same function. So, at least, one of three SYNC pins operates as SYNC<sup>TM</sup> function, TS04P can be operated with other TS04P or TSxx series without interfering with each other. Inside of TS04P, there is internal oscillator for SYNC pulse so no external component is used for SYNC<sup>TM</sup> function. Simply, it is needed to connect SYNC pin to other SYNC pin of TS04P or TSxx series for using SYNC<sup>TM</sup> function. For proper SYNC<sup>TM</sup> function, less five other TS04P or TSxx series can be connected with.









#### 8.3.2 Sensitivity selections

SYNC1 and SYNC2 pin of TS04P can be used as sensitivity selection pin. Both of two SYNC pins have three methods of connection. Open connection (N.C., SYNC connection), connection to GND, and connection to VDD are these methods. As below table, TS04P has 9 step sensitivity selections. When SYNC1 pin or SYNC 2 pin has no connection to GND or VDD, that SYNC pin may be simultaneously used for SYNC<sup>TM</sup> function.

Sensitivity level (thickness [mm] of proper poly-carbonate insulator) of each sensitivity selection

| SYNC1<br>SYNC2         | Connect to VDD | Connect to GND | N.C.<br>(SYNC connection) |
|------------------------|----------------|----------------|---------------------------|
| Connect to GND         | 15.0           | 13.0           | 11.0                      |
| N.C. (SYNC connection) | 9.0            | 7.5            | 6.0                       |
| Connect to VDD         | 5.0            | 4.0            | 3.0                       |

Note 3: The size of touch PAD is 10 mm x 7 mm used.

Note 4: Above proper thickness is reliable but it can be changed by insulator material and application.

#### 8.3.3 Output mode selections

SYNC3 pin of TS04P is output mode selection input pin. SYNC3 also has three connections, such as open connection (N.C., SYNC connection), connection to GND, and connection to VDD. The output mode of each connection is such as below table.

Output mode of each SYNC3 connections

| SYNC3 connection | Connect to VDD | Connect to GND | N.C.<br>(SYNC connection) |  |
|------------------|----------------|----------------|---------------------------|--|
| Output mode      | Single output  | Multi-output   | Single output             |  |

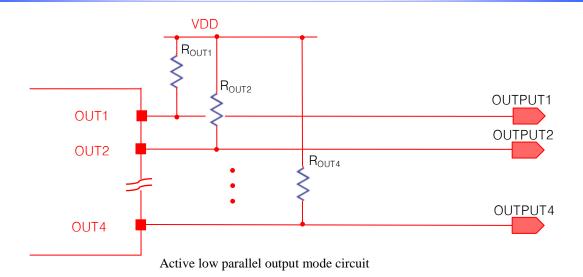
TS04P operates as single output mode when SYNC3 is connected to VDD or open, the one output that is detected fastest is appeared. So application PCB composed very near touch pads is possible to operate without confusion of neighborhood touch. When SYNC3 is connected to GND and TS04P operates as multi-output mode, all output of TS04P can be appeared.

#### 8.4 Parallel output

TS04P acts as active low parallel output mode. Parallel output ports (OUT1 ~ OUT4) have an open drain NMOS structure. For this reason, the parallel output mode of TS04P needs  $R_{OUT}$  as below figures. The maximum output drive current is 4mA, so over a few  $k\Omega$  must be used as  $R_{OUT}$ . Normally  $10k\Omega$  is used as  $R_{OUT}$ .







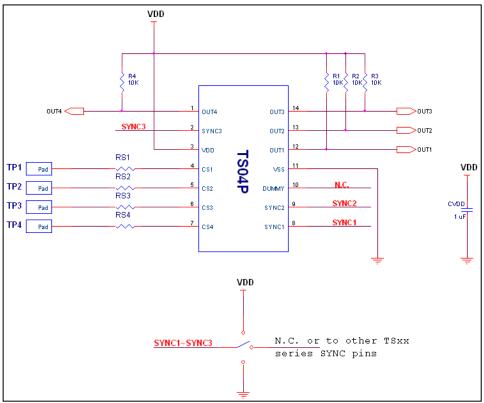
### 8.5 Internal reset operation

The TS04P has stable internal reset circuit to offer reset pulse to digital block. The supply voltage for a system start or restart should be under 0.3·VDD of normal operation VDD. No external components required for TS04P power reset, that helps simple circuit design and to realize the low cost application.





### 9 Recommended Circuit Diagram



TS04P Application Example Circuit

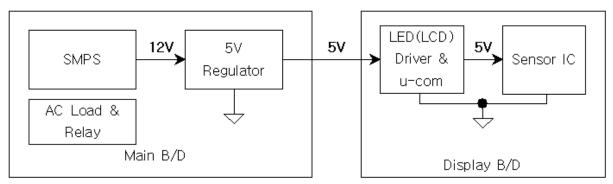
- ✓ TS04P is reset by internal reset circuit. VDD voltage rising time should be shorter than 100msec for proper operation.
- ✓ Normally, DUMMY pin dose not connection to anywhere. But, in radio frequency noise environment, DUMMY pin must form a pattern line on PCB.
- ✓ The VDD periodic voltage ripple over 50mV and the ripple frequency is lower than 10 kHz can cause wrong sensitivity calibration. To prevent above problem, power (VDD, GND) line of touch circuit should be separated from other circuit. Especially LED driver power line or digital switching circuit power line certainly should be treated to be separated from touch circuit.
- ✓ The CS patterns also should be routed as short as possible and the width of line might be about 0.25mm.
- ✓ Parallel capacitor of CS pin could be useful in case detail sensitivity mediation is required such as for complementation sensitivity difference between channels.
- ✓ Serial connection resistor of CS pins may be used to avoid mal-function from external surge and ESD and the closer to IC(TS04P), the stronger immunity against mal-function and ESD is.
- ✓ The capacitor that is between VDD and GND is an obligation. It should be located as close as possible from TS04P.
- ✓ The CS pattern routing should be formed by bottom metal (opposite metal of touch PAD).
- ✓ The empty space of PCB must be filled with GND pattern to strengthen GND pattern and to prevent external noise from interfere with sensing frequency.





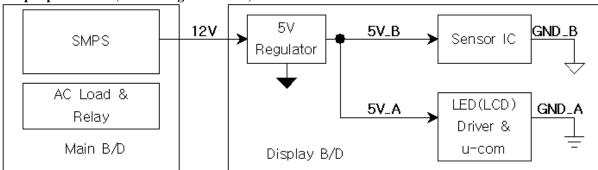
#### 9.1 Example - Power Line Split Strategy PCB Layout

#### A. Not split power Line (Bad power line design)

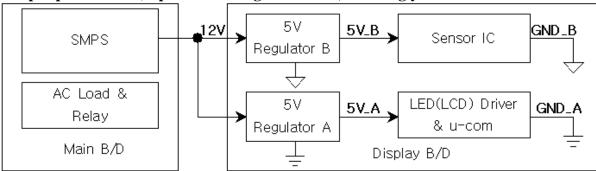


- The The noise that is generated by AC load or relay can be loaded at 5V power line.
- A big inductance might be appeared in case of the connection line between main board and display board is too long, moreover the voltage ripple could be generated by LED (LCD) display driver at VDD (5V).

#### B. Split power Line (One 5V regulator used) - Recommended



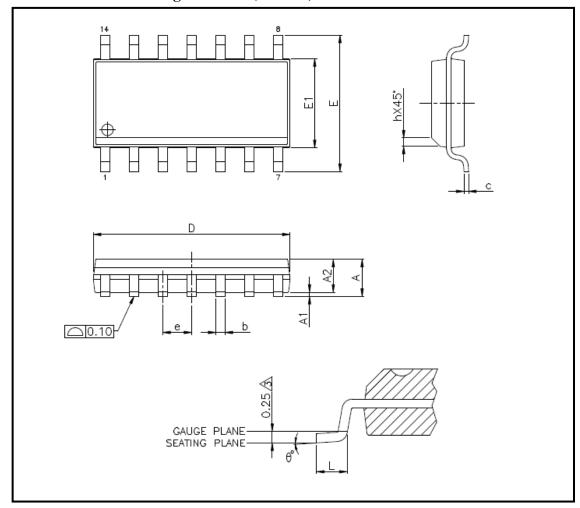
#### C. Split power Line (Separated 5V regulator used) – Strongly recommended





### 10 MECHANICAL DRAWING

#### 10.1 Mechanical Drawing of TS04P (14 SOP)







| SYMBOLS | MIN.     | MAX. |  |
|---------|----------|------|--|
| Α       | l        | 1.75 |  |
| A1      | 0.10     | 0.25 |  |
| A2      | 1.25     |      |  |
| Ь       | 0.31     | 0.51 |  |
| С       | 0.10     | 0.25 |  |
| D       | 8.65 BSC |      |  |
| E       | 6.00 BSC |      |  |
| E1      | 3.90     | BSC  |  |
| e       | 1.27     | BSC  |  |
| L       | 0.40     | 1.27 |  |
| h       | 0.25     | 0.50 |  |
| θ°      | 0        | 8    |  |

UNIT: mm

#### NOTES:

1.JEDEC OUTLINE: MS-012 AB REV.F
2.DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH,
PROTRUSIONS OR GATE BURRS.MOLD FLASH, PROTRUSIONS
AND GATE BURRS SHALL NOT EXCEED 0.15mm.

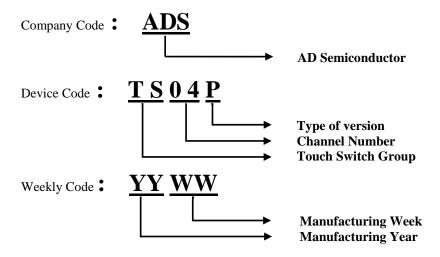
3.DIMENSIONS "E1" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25mm PER SIDE.





### 11 MARKING DESCRIPTION

#### 11.1 Marking Description of TS04P







| N | $\cap$ | TE | ٦. |
|---|--------|----|----|

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